

# BUK9MFF-65PSS

Dual TrenchPLUS FET Logic Level FET

Rev. 04 — 17 June 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

### 1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

### 1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

### 1.4 Quick reference data

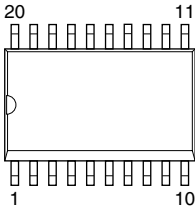
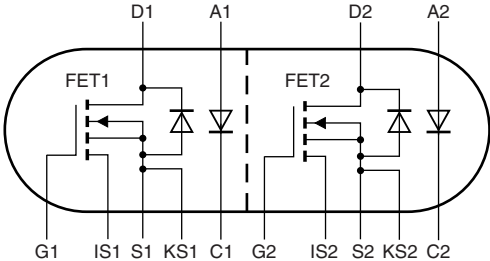
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>FET1 and FET2 static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 16</a>	-	11.4	13.4	m $\Omega$
$I_D/I_{sense}$	ratio of drain current to sense current	$T_j = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 17</a>	5831	6479	7127	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$	65	-	-	V



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 <p><b>SOT163-1 (SO20)</b></p>	 <p style="text-align: right;">003aaa745</p>
2	IS1	current sense 1		
3	D1	drain		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9MFF-65PSS	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>FET1 and FET2</b>							
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$ ; $25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V	
$V_{GS}$	gate-source voltage		-15	-	15	V	
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	[1][2]	-	-	13.6	A
		$V_{GS} = 5\text{ V}$ ; $T_{sp} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	[1][2]	-	-	8.6	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; single pulse; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 4</a>	-	-	272.1	A	
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	4.75	W	
$T_{stg}$	storage temperature		-55	-	150	°C	
$T_j$	junction temperature		-55	-	150	°C	
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	-	100	V	
<b>FET1 and FET2 source-drain diode</b>							
$I_S$	source current	$T_{sp} = 25\text{ °C}$	[1][2]	-	-	13.6	A
$I_{SM}$	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{sp} = 25\text{ °C}$	-	-	272	A	
<b>FET1 and FET2 avalanche ruggedness</b>							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 13.6\text{ A}$ ; $V_{sup} = 65\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; see <a href="#">Figure 3</a>	[3][4][5]	-	-	702	mJ
<b>FET1 and FET2 electrostatic discharge</b>							
$V_{ESD}$	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$ ; all pins	-	-	0.15	kV	
		HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$ ; pins 8, 11 and 15 to pins 6, 7, 12, 13 and 14 shorted	-	-	4	kV	
		HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$ ; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted	-	-	4	kV	

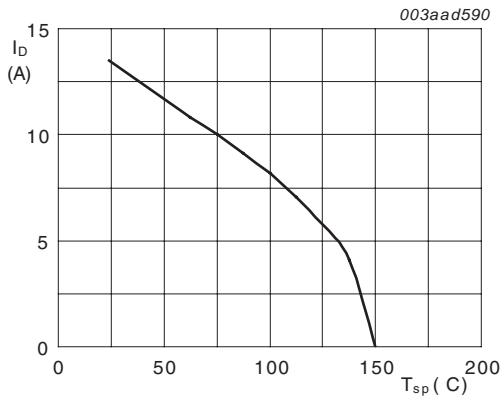
[1] Single device conducting.

[2] Current is limited by chip power dissipation rating.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

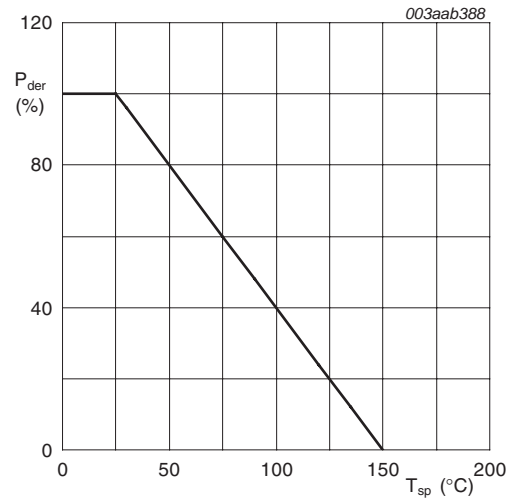
[4] Repetitive rating defined in avalanche rating figure.

[5] Refer to application note AN10273 for further information.



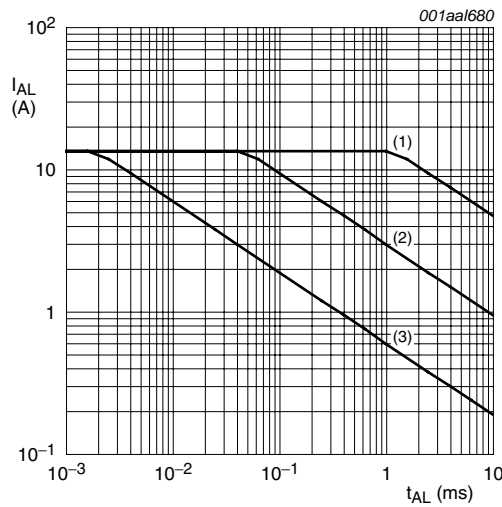
$$V_{GS} \geq 5 V$$

**Fig 1. Continuous drain current as a function of solder point temperature, FET1 and FET2**



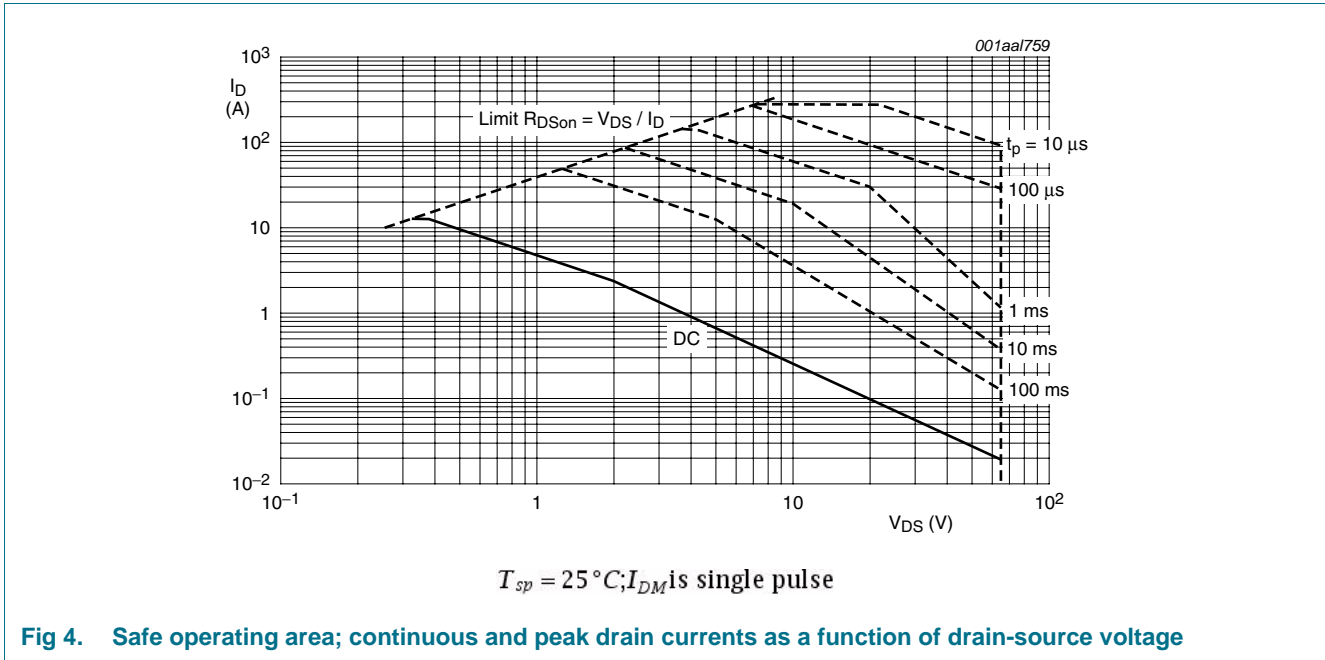
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature, FET1 and FET2**



- (1) Single-pulse;  $T_j = 25^{\circ}C$ .
- (2) Single-pulse;  $T_j = 150^{\circ}C$ .
- (3) Repetitive.

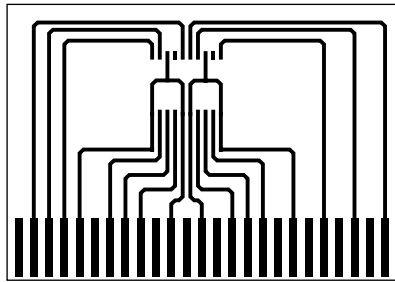
**Fig 3. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.**



## 5. Thermal characteristics

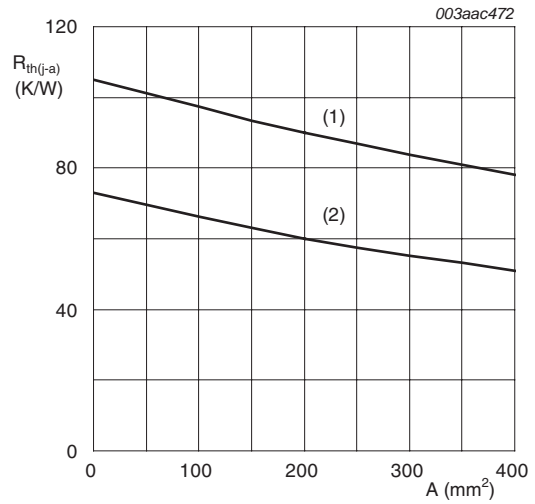
**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	26	K/W
		FET2	-	-	26	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; both channels conducting; zero heat sink area; see <a href="#">Figure 5</a> ; see <a href="#">Figure 6</a>	-	73	-	K/W
		mounted on a printed-circuit board; both channels conducting; 200 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 7</a> ; see <a href="#">Figure 6</a>	-	60	-	K/W
		mounted on a printed-circuit board; both channels conducting; 400 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 8</a> ; see <a href="#">Figure 6</a>	-	51	-	K/W
		mounted on a printed-circuit board; one channel conducting; zero heat sink area; see <a href="#">Figure 5</a> ; see <a href="#">Figure 6</a>	-	105	-	K/W
		mounted on a printed-circuit board; one channel conducting; 200 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 7</a> ; see <a href="#">Figure 6</a>	-	90	-	K/W
		mounted on a printed-circuit board; one channel conducting; 400 mm <sup>2</sup> copper heat sink area; see <a href="#">Figure 8</a> ; see <a href="#">Figure 6</a>	-	70	-	K/W



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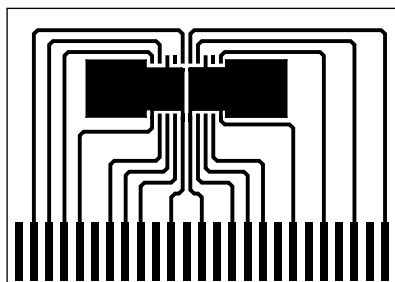
Fig 5. PCB used for thermal tests; zero heat sink area



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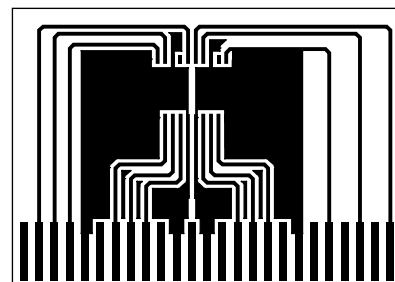
- (1) One channel conducting dissipating 500mW.
  - (2) Both channels conducting each dissipating 500mW.
- Zero air flow

Fig 6. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area



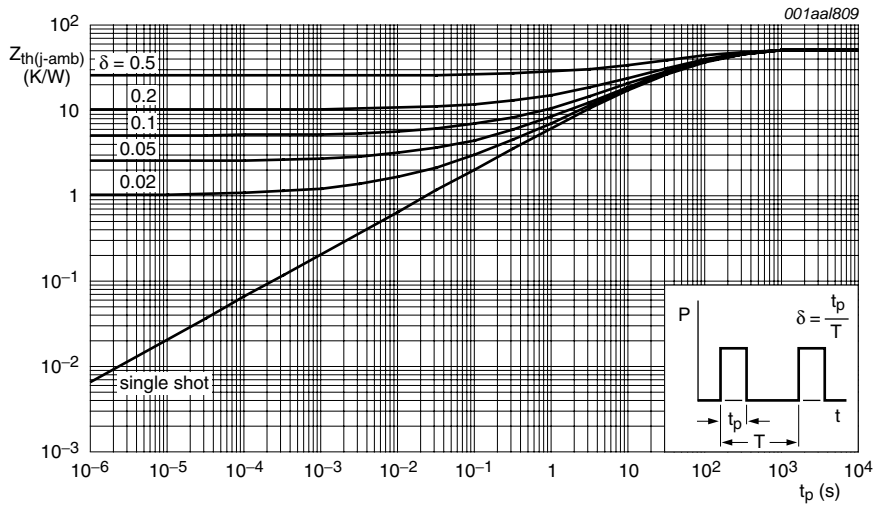
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Fig 7. PCB used for thermal tests; heat sink area 200 mm²



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Fig 8. PCB used for thermal tests; heat sink area 400 mm²



**Fig 9. Transient thermal impedance from junction to ambient as a function of pulse duration, FET1 and FET2**



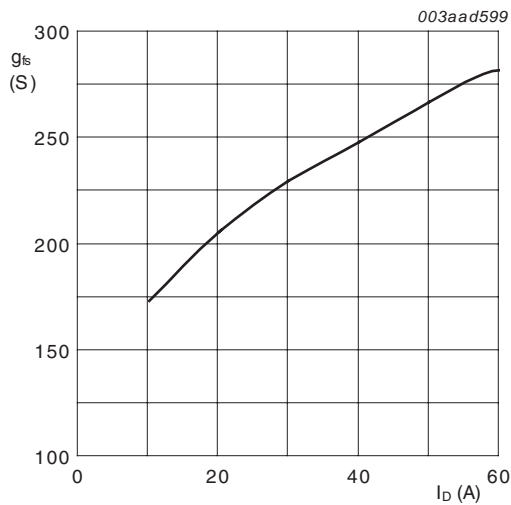
## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>FET1 and FET2 static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	65	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	59	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	3	$\mu\text{A}$
		$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	125	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	300	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 16</a>	-	11.4	13.4	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 16</a>	-	-	25.5	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 16</a>	-	-	14.7	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 16</a>	-	-	12.3	m $\Omega$
$I_D/I_{sense}$	ratio of drain current to sense current	$V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 17</a>	5831	6479	7127	A/A
$S_F(TSD)$	temperature sense diode temperature coefficient	$I_F = 250 \mu\text{A}; 25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 18</a>	-5.4	-5.7	-6	mV/K
$V_F(TSD)$	temperature sense diode forward voltage	$I_F = 250 \mu\text{A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 18</a>	2.855	2.9	2.945	V
<b>FET1 and FET2 dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 52 \text{ V}; V_{GS} = 5 \text{ V};$ see <a href="#">Figure 19</a>	-	40.2	-	nC
$Q_{GS}$	gate-source charge		-	8.48	-	nC
$Q_{GD}$	gate-drain charge		-	16.8	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 20</a>	-	3052	-	pF
$C_{oss}$	output capacitance		-	416	-	pF
$C_{riss}$	reverse transfer capacitance		-	186	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 3 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega$	-	37	-	ns
$t_r$	rise time		-	64	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 30 \text{ V}; V_{GS} = 5 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega$	-	151	-	ns
$t_f$	fall time	$V_{DS} = 30 \text{ V}; R_L = 3 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega$	-	78.14	-	ns
$L_D$	internal drain inductance	from pin to center of die	-	0.9	-	nH
$L_S$	internal source inductance	from source lead to source bonding pad	-	2	-	nH

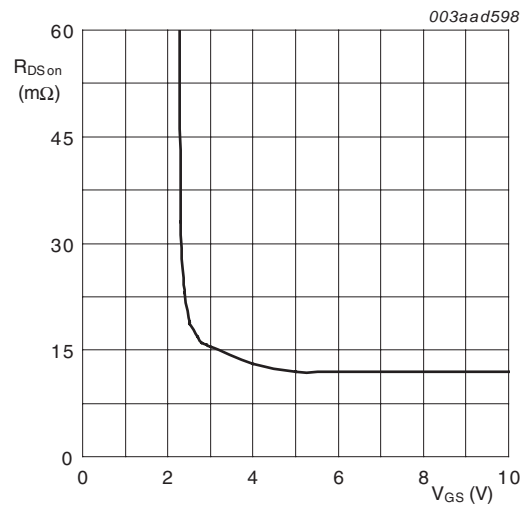
**Table 6. Characteristics ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>FET1 and FET2 source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 21</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	51	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$	-	0.127	-	nC



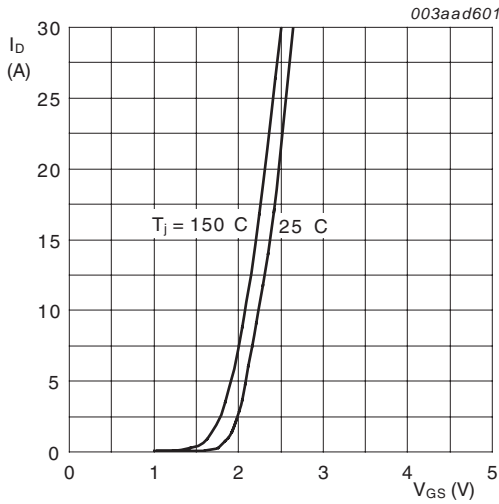
$T_j = 25\text{ °C}$ ;  $V_{DS} = 25\text{ V}$

**Fig 10. Forward transconductance as a function of drain current; typical values, FET1 and FET2**

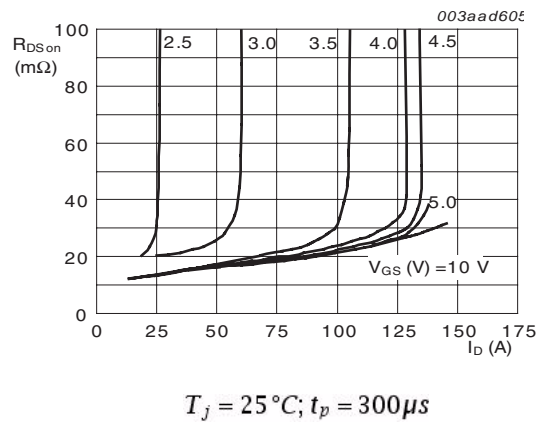


$T_j = 25\text{ °C}$ ;  $I_D = 10\text{ A}$

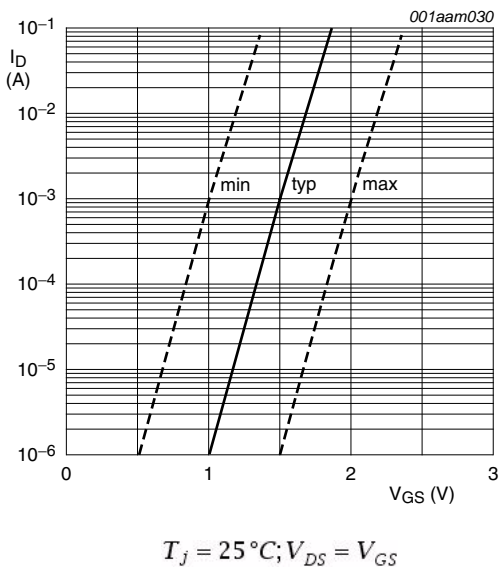
**Fig 11. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2**



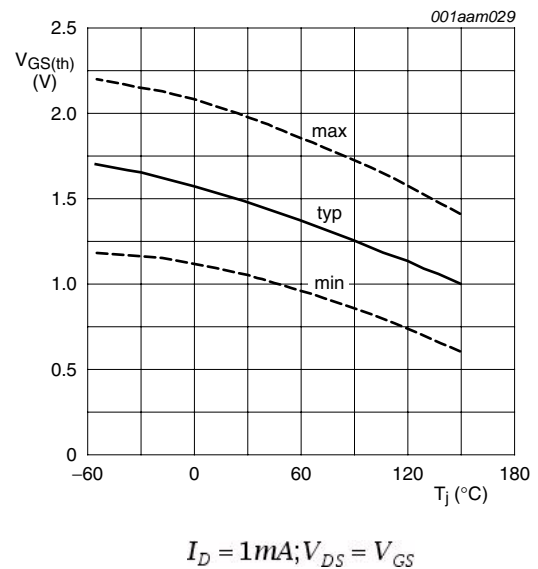
**Fig 12. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2**



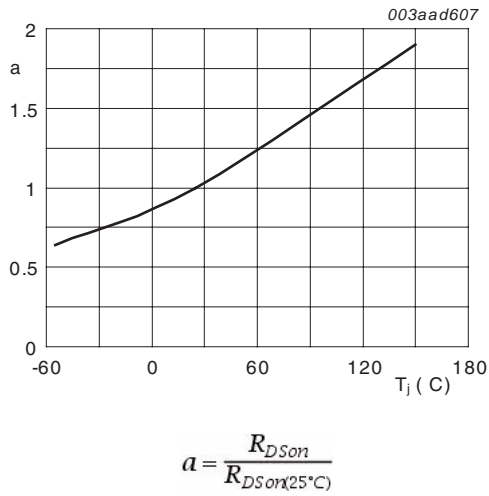
**Fig 13. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2**



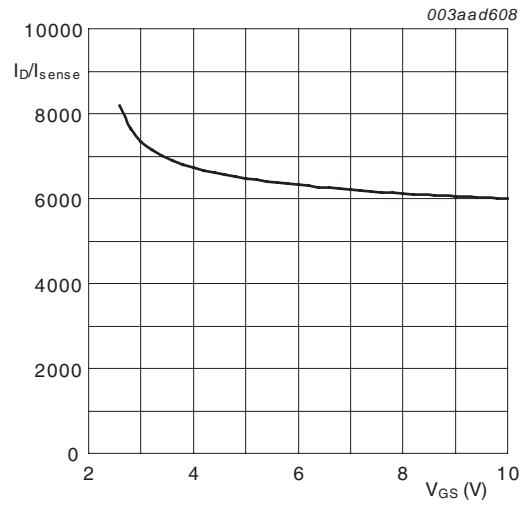
**Fig 14. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2**



**Fig 15. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2**

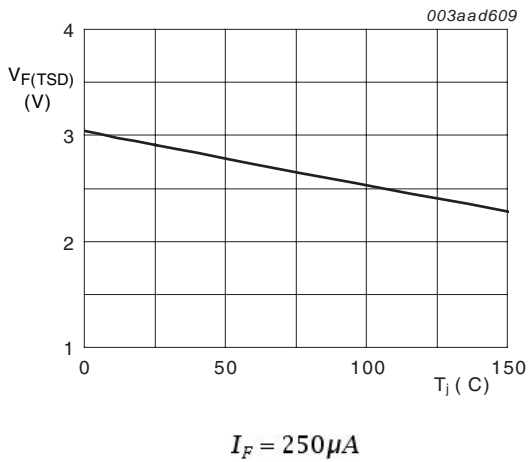


**Fig 16. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2**

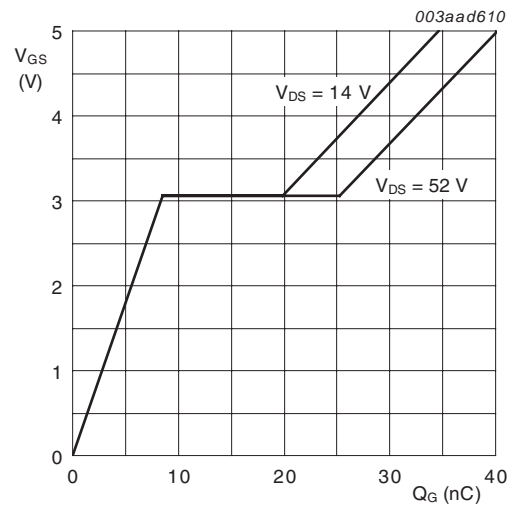


$T_j = 25^{\circ}C; I_D = 5A$

**Fig 17. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2**

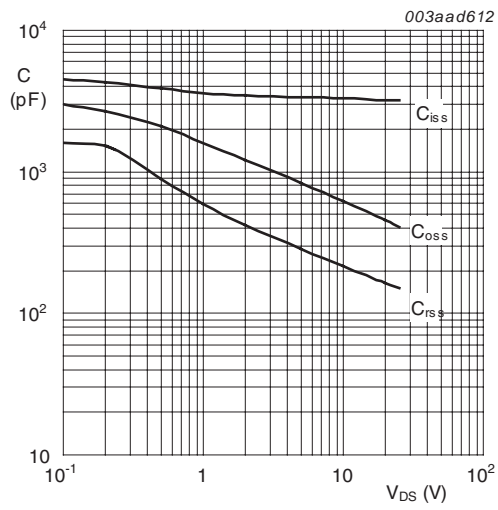


**Fig 18. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2**



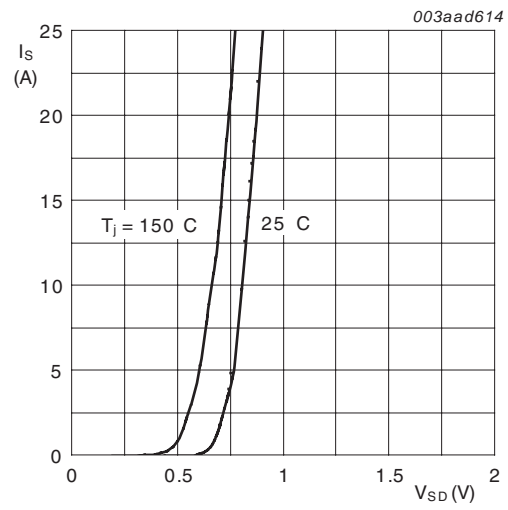
$T_j = 25^{\circ}C; I_D = 10A$

**Fig 19. Gate-source voltage as a function of turn-on gate charge; typical values, FET1 and FET2**



$V_{GS} = 0V; f = 1MHz$

**Fig 20. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2**



$V_{GS} = 0V$

**Fig 21. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2**

**7. Package outline**

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

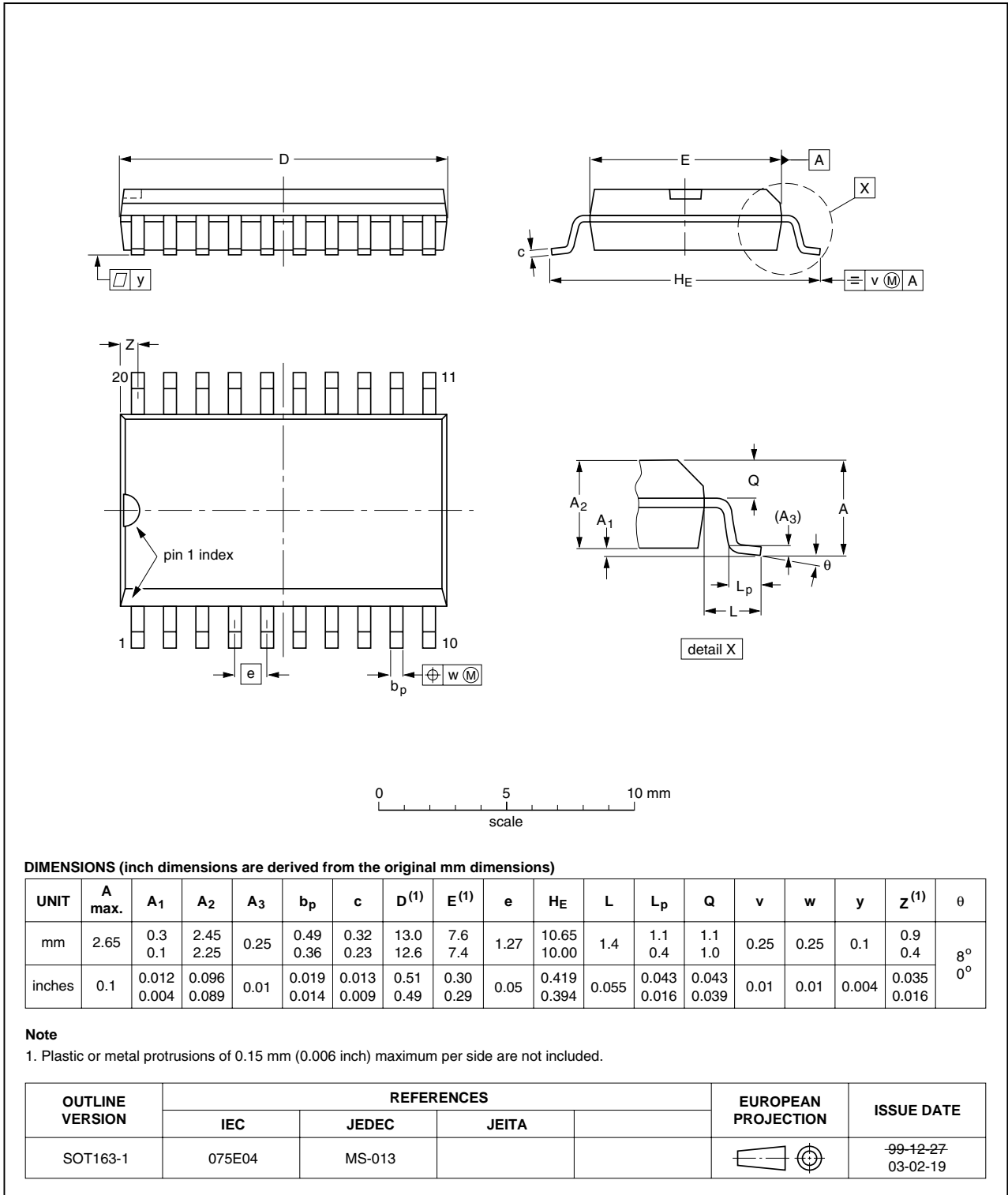


Fig 22. Package outline SOT163-1 (SO20)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MFF-65PSS v.4	20100617	Product data sheet	-	BUK9MFF-65PSS v.3
Modifications:		<ul style="list-style-type: none"><li>• Status changed from preliminary to product.</li><li>• Various changes to content.</li></ul>		
BUK9MFF-65PSS v.3	20100531	Preliminary data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 10. Contact information

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